

Application No. 09/928,402
Attorney Docket No. 4100-0130P

CLAIM SET AS AMENDED

1. A method for estimating one of the frequency (f_{a1}) and the phase (ϕ_{a1}) of a digital input signal ($x(i)$) having the following process steps:
 - determining phase values ($C_{a1}(i)$) of the digital input signal ($x(i)$),
 - summing the phase values ($C_{a1}(i)$) over a predetermined summation length N/B which is a predetermined fraction $1/B$ of an observation length of N phase values ($C_{a1}(i)$), to create added-up phase values ($S_{a1}(i)$),
 - reducing a sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with a sampling rate (f_{a2}) of the phase values ($C_{a1}(i)$),
 - delaying the added-up phase values ($S_{a1}(i)$) with at least $B-1$ delay elements, each of which delays the added-up phase values ($S_{a1}(i)$) by one sampling period of the reduced sampling rate ($f_{a2} \cdot B/N$),
 - adding up the delayed added-up phase values ($S_{a1}(i)$) to create a resulting pulse response (h_f) of the frequency so that one of the resulting pulse responses (h_f) of the frequency (f_{a1}) is constant positive in a first interval, is zero in a second interval, and is constant negative in a

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third interval (42), and such that a resulting pulse response (h_p) of the phase is constant in at least a middle interval of the observation length and is otherwise zero.

2. (currently amended) The method of claim 1, wherein the fraction $1/B$ is $1/(3 \cdot n)$, where n is a positive integer.
3. The method of claim 2, wherein the fraction $1/B$ is $1/3$, wherein a first delay element and second delay element are provided, and wherein the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element is subtracted from the added-up phase value ($S_{a1}(i)$) at the input of the first delay element to determine the estimated frequency (f_{a1}).
4. The method of claim 2, wherein the fraction $1/B$ is $1/3$, wherein a first delay element and second delay element are provided, and wherein the added-up phase value ($S_{a1}(i)$) at the input of the first delay element, the added-up phase value ($S_{a1}(i)$) at the output of the first delay element, and the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element are summed to determine the estimated phase (ϕ_{a1}).

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5. The method of claim 2, wherein the fraction $1/B$ is $1/6$, wherein a first, second, third, fourth, and fifth delay elements are provided, and wherein the added-up phase value at the input of the first delay element and the added-up phase value ($S_{a1}(i-1)$) at the output of the first delay element are added, and from this the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element and ($S_{a1}(i-5)$) at the output of the fifth delay element are subtracted to determine the estimated frequency (f_{a1}).

6. The method of claim 2, wherein the fraction $1/B$ is equal to $1/6$, wherein a first, second, third, fourth, and fifth delay elements are provided, and the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element, ($S_{a1}(i-2)$) at the output of the second delay element, ($S_{a1}(i-3)$) at the output of the third delay element and ($S_{a1}(i-4)$) at the output of the fourth delay element are summed to determine the estimated phase (ϕ_{a1}).

7. The method of claim 1, wherein each of the first interval, the second interval, and the third interval of the resulting pulse response (h_f) of the frequency has a length of N/B , in particular $1/3 N$.

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8. The method of claim 1, wherein the middle interval of the resulting pulse response (h_ϕ) of the phase has the length $N \cdot (3n-n)/3 \cdot n$, in particular $2/3 N$, where n is a positive integer.

9. The method of claim 1, wherein the middle interval of the resulting pulse response (h_ϕ) extends over the total observation length N .

10. An apparatus for estimating the frequency (f_{a1}) and/or the phase (ϕ_{a1}) of a digital input signal ($x(i)$), the apparatus comprising:

- a phase determining device, which determines phase values ($C_{a1}(i)$) of the digital input signal ($x(i)$),
- a first filter, which adds up the phase values ($C_{a1}(i)$) over a predetermined summation length N/B , which is a predetermined fraction $1/B$ of an observation length of N phase values ($C_{a1}(i)$), to form added-up phase values ($S_{a1}(i)$), and the sampling rate of the added-up phase values ($S_{a1}(i)$) is reduced by a factor N/B in comparison with a sampling rate (f_{a2}) of the phase values ($C_{a1}(i)$),
- a second filter which delays the added-up phase values

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($S_{a1}(i)$) in a chain of at least $B-1$ delay elements, which respectively delay the added-up phase values ($S_{a1}(i)$) by one sampling period of the reduced sampling rate ($f_{a2} \cdot B/N$), and adds or subtracts the delayed added-up phase values ($S_{a1}(i)$) to create a resulting pulse response (h_f) of the frequency so that at least one of: a resulting pulse response (h_f) of the frequency is constant positive in a first interval, is zero in a second interval, or is constant negative in a third interval, and wherein a resulting pulse response (h_ϕ) of the phase is created so that the resulting pulse response (h_ϕ) of the phase is constant in at least a middle interval and is otherwise zero.

11. The apparatus of claim 10, wherein the phase determination device has a counter whose count is read out at a constant sampling rate (f_{a2}).

12. The apparatus of claim 10, wherein the first filter has an integrator, a differentiator and a first sampling-rate converter arranged between the integrator and the differentiator to reduce the sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with the sampling rate frequency (f_{a2}) of the phase values

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$(C_{a1}(i))$.

13. The apparatus of claim 10, wherein the fraction $1/B$ is $1/3$, and the second filter has a first delay element and a second delay element and a subtractor, which subtracts the added-up phase values $(S_{a1}(i-2))$ at the output of the second delay element from the added-up phase values $(S_{a1}(i))$ at the input of the first delay element to determine the estimated frequency (f_{a1}) .

14. The apparatus of claim 10, wherein the fraction $1/B$ is $1/3$, and the second filter has a first delay element and a second delay element and adders which sum the added-up phase values $(S_{a1}(i))$ at the input of the first delay element, the added-up phase values $(S_{a1}(i-1))$ at the output of the first delay element, and the added-up phase values $(S_{a1}(i-2))$ at the output of the second delay element to determine the estimated phase (ϕ_{a1}) .

15. The apparatus of claim 13, wherein a second sampling-rate converter is arranged to follow at least one of the adders and the subtractor to reduce the sampling rate by a factor of 3.

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16. The apparatus of claim 10, wherein the fraction $1/B$ is $1/6$, and the second filter has a first, second, third, fourth, and fifth delay elements, an adder that adds up the added-up phase values $(S_{a1}(i))$ at the input of the first delay element and the added-up phase values $(S_{a1}(i-1))$ at the output of the first delay element, and subtractors which subtract therefrom the added-up phase values $(S_{a1}(i-4))$ at the output of the fourth delay element and the added-up phase values $(S_{a1}(i-5))$ at the output of the fifth delay element to determine the estimated frequency (f_{a1}) .

17. The apparatus of claim 10, wherein the fraction $1/B$ is $1/6$, and the second filter has a first, second, third, fourth, and fifth delay elements and adders which add up the added-up phase values $(S_{a1}(i-1))$ at the output of the first delay element, the added-up phase values $(S_{a1}(i-2))$ at the output of the second delay element, the added-up phase values $(S_{a1}(i-3))$ at the output of the third delay element and the added-up phase values $(S_{a1}(i-4))$ at the output of the fourth delay element to determine the estimated phase (ϕ_{a1}) .

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18. The apparatus of claim 16, wherein a second sampling-rate converter is respectively arranged after at least one of the adders and the subtractors for reducing the sampling rate by a factor of 6.